Màster en

Enginyeria de Semiconductors i Disseny Microelectrònic

Comitè acadèmic:

Dra. Núria Barniol, Universitat Autònoma de Barcelona

Dr. Xavier Muñoz, Centre Nacional de Microelectrònica

Dr. Antonio Rubio, Universitat Politècnica de Catalunya

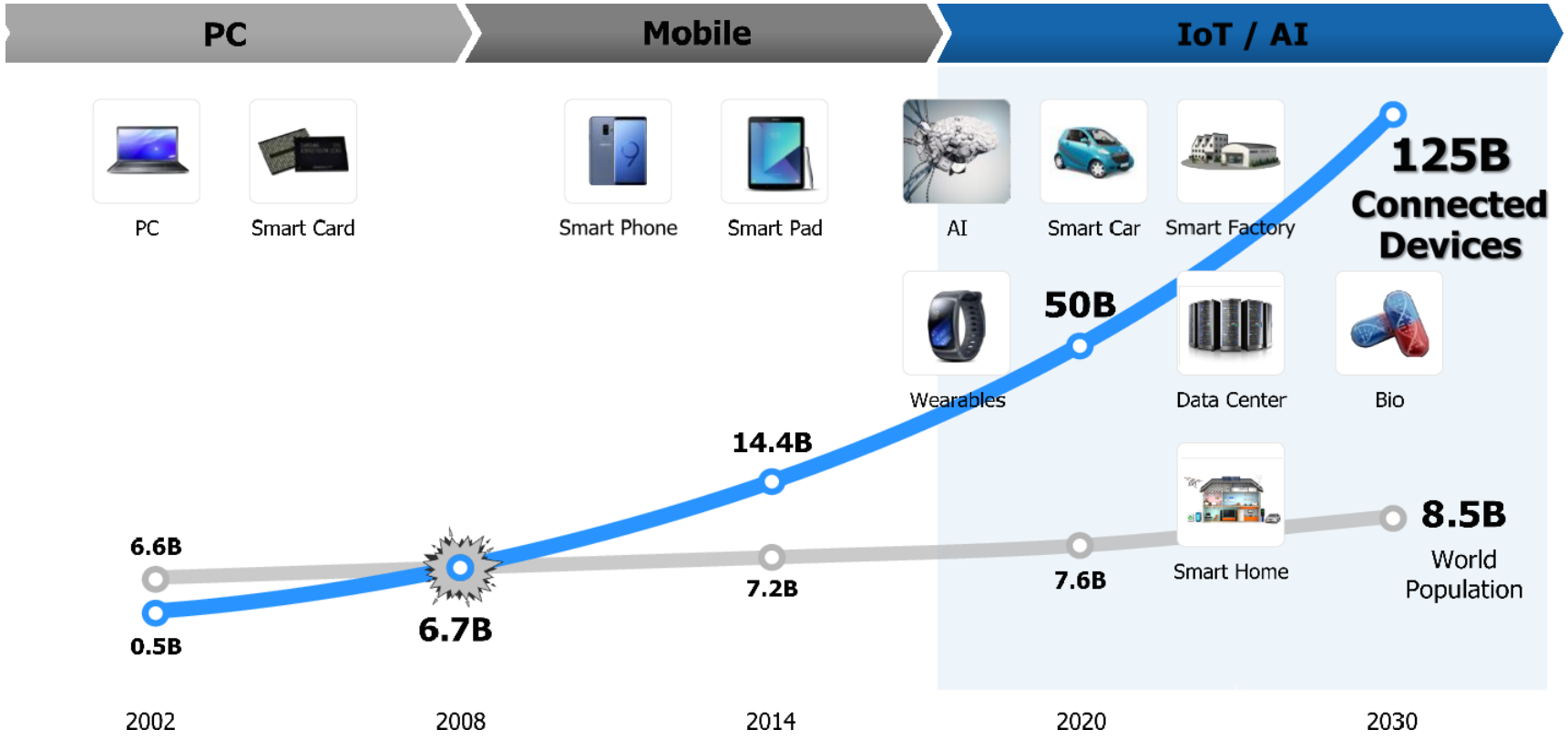
Dr. Albert Cirera, Universitat de Barcelona

Dr. Benjamín Íñiguez, Universitat Rovira i Virgili

- Per què?

Justificació dels nous estudis

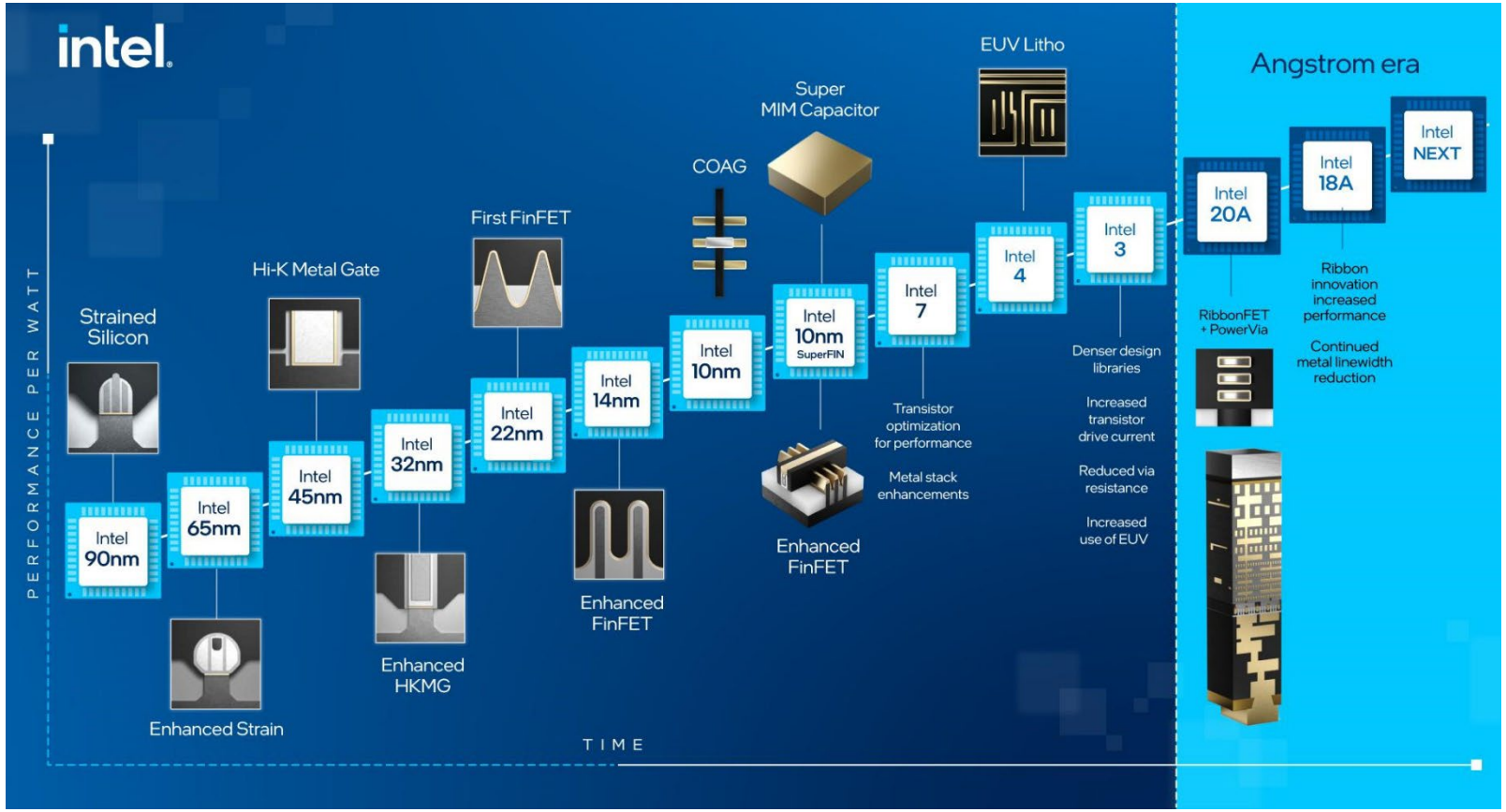
CISCO augura per 2030 125B de interconexions a internet, en camps d'aplicació com la seguretat, l'energía, la salut, amb el rol del núvol.



Activitats com el Internet de les coses (IoT) o la Inteligència Artificial (IA) pronostican que las aplicacions i el consequent mercat al voltant de la Electrònica Integrada i els Computadors marcaran el progrés I, en gran part, la sobirania dels països.

Justificació dels nous estudis

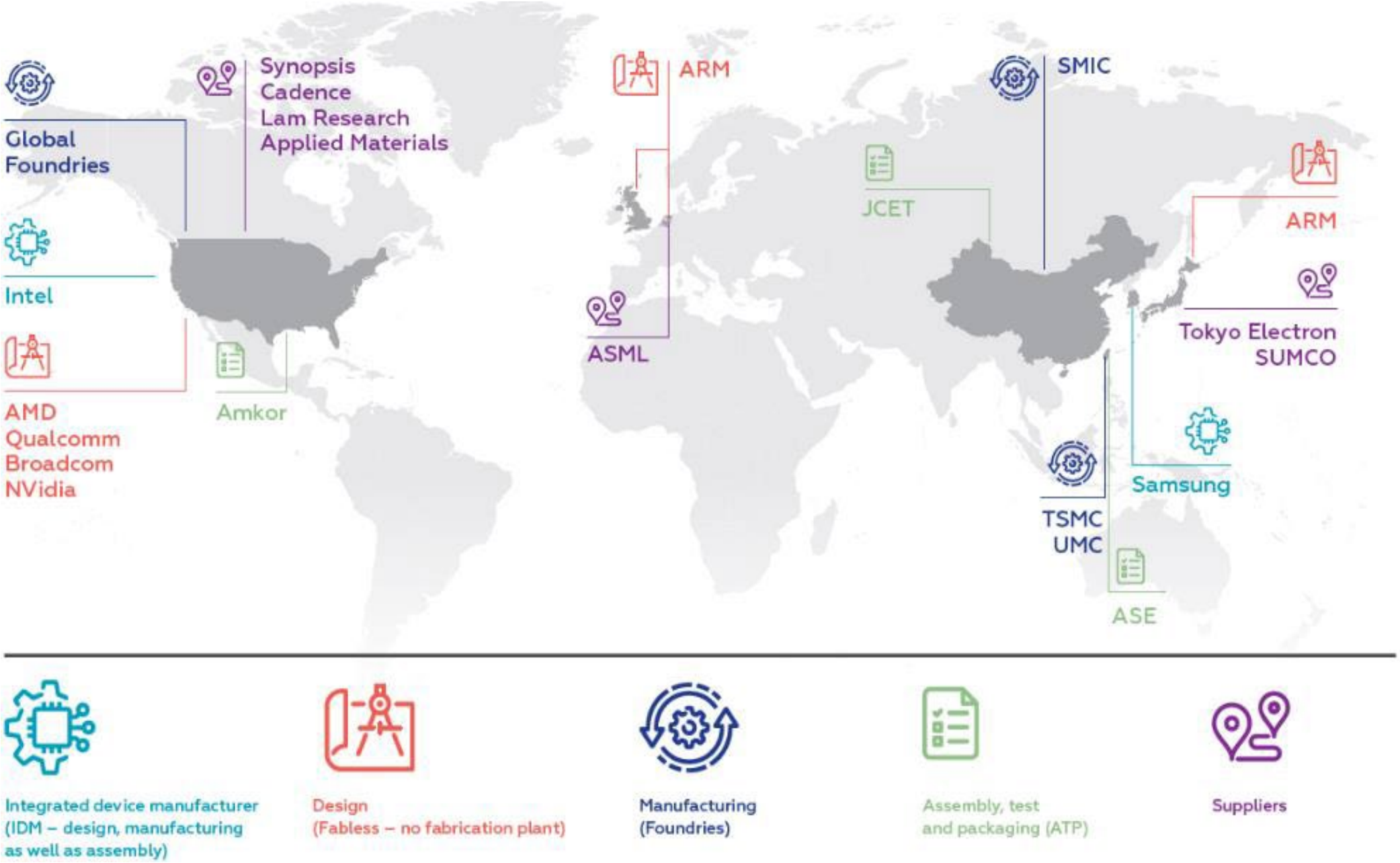
La tecnología dels circuits integrats segueix una forta evolución: La Llei de Moore



Today

3 nm

Però les uniques empreses amb capacitat de fabricar circuits sofisticats son TSMC i Samsung (+Intel).


Global Foundries
Synopsis
Cadence
Lam Research
Applied Materials
Intel
AMD
Qualcomm
Broadcom
NVidia
Amkor
ARM
ASML
JCET
SMIC
ARM
Tokyo Electron
SUMCO
Samsung
TSMC
UMC
ASE
Integrated device manufacturer (IDM – design, manufacturing as well as assembly)
Design (Fabless – no fabrication plant)
Manufacturing (Foundries)
Assembly, test and packaging (ATP)
Suppliers

Justificació dels nous estudis

Els paisos han reaccionat a la gran oferta de riquesa i treball que la tecnología del CIs comporta, accelerada per la necessitat d'assegurar la sobirania nacional

The European Chips Act will bolster Europe's competitiveness and resilience in semiconductor technologies and applications, and help achieve both the digital and green transition. It will do this by strengthening Europe's technological leadership in the field. Following the approval by the Parliament and the Council, the regulation entered into force on 21 September 2023.

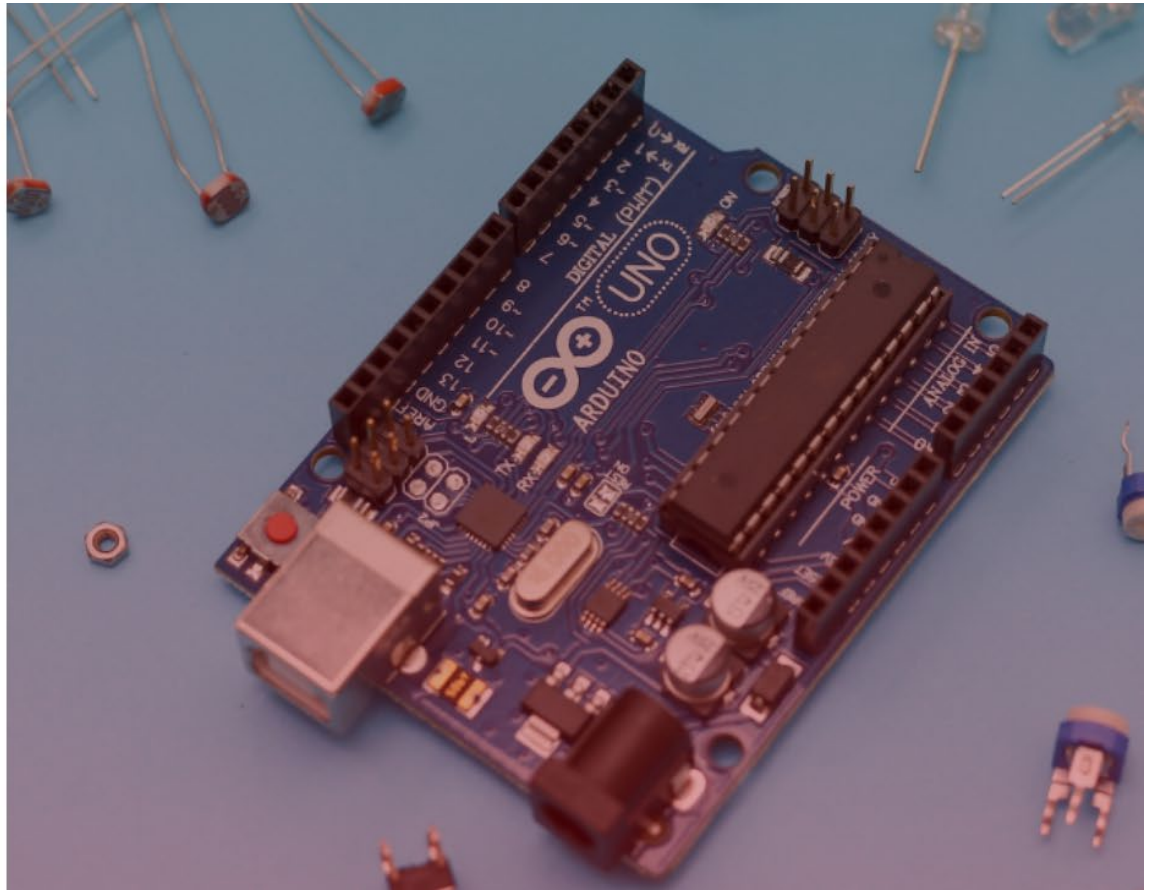
Que passa a Espanya?

Que passa a Espanya?

El proyecto para convertir a España en un referente en el diseño y fabricación de Chips

En plena transformación digital del país, el Gobierno ha puesto en marcha el Proyecto Estratégico de Microelectrónica y Semiconductores, conocido como PERTE Chip, para desarrollar toda la cadena de valor de la industria a partir de las fortalezas existentes.

Se articula en torno a 4 ejes, a partir de las fortalezas nacionales, para reforzar las capacidades de diseño y producción de microchips en España. Se trata de un plan-país ambicioso y financiado con fondos Next Generation EU.



I a Catalunya?

- Catalunya és referent en fabricació de circuits de Silici,

Centre Nacional de Microelectrònica

- Catalunya és referent en disseny de processadors avançats

Centre Nacional de Supercomputació (BSC)

- Catalunya és referent en recerca en l'àrea, UPC, UB, UAB
- Catalunya és referent en formació en l'àrea, UPC, UB, UAB
- Catalunya atrau companyies i està consolidant un eco-Sistema en l'àrea

Ranking QS 2023, Electrical and Electronics

Rank	University	Overall Score	
58	Universitat Politècnica de Catalunya · BarcelonaTech (UPC) Barcelona, Spain	75.4	Shortlist
151-200	Universitat Autònoma de Barcelona Barcelona, Spain More Details	n/a	Shortlist
151-200	Universitat de Barcelona Barcelona, Spain	n/a	Shortlist

Ranking QS 2023, Physics

Rank	University	Overall Score	
85	Universitat de Barcelona Barcelona, Spain	75.8	Shortlist
115	Universitat Autònoma de Barcelona Barcelona, Spain More Details	73.6	Shortlist
151-200	Universitat Politècnica de Catalunya · BarcelonaTech (UPC) Barcelona, Spain	n/a	Shortlist


"Integrated Micro and Nanofabrication Clean Room of CNM"
Large Scale Facility of MINECO
ICTS-SBCNM
ICTS cleanroom
Contact
Instituto de Microelectrónica de Barcelona IMB-CNM
Centro Nacional de Microelectrónica
CAMPUS UAB
08193 - Cerdanyola del Vallès - Barcelona - Spain
icts@imb-cnm.csic.es
Tel. +34 594 77 00
www.imb-cnm.csic.es/icts
Fax. +34 580 02 67
1500 m2

Media

ara

Universitats i centres de recerca i tecnològics catalans creen un clúster de formació en nanoelectrònica i microxips

LA VANGUARDIA

Crean en Cataluña un clúster de formación en nanoelectrónica y microchips

Crean en Cataluña un clúster de formación en nanoelectrónica y microchips

COPE

Universitats i centres de recerca i tecnològics creen un clúster de formació en nanoelectrònica i microxips

La República

Universidades y centros de investigación y tecnológicos crean un clúster de formación en nanoelectrónica y microchips

myScience

Apoyo científico a que Cataluña acoja fábrica de semiconductores y microchips

estrella DIGITAL

CincoDías

EL PAÍS ECONOMÍA

Compañías Mercados Economía Mi Dinero Fortuna / Cotizaciones

Compañías

TECNOLOGÍA >

Intel invertirá en Barcelona 200 millones en 10 años

- El laboratorio de microchips dará empleo a 300 trabajadores

Industria

La empresa de semiconductores MPS contratará 150 ingenieros en Barcelona

* *La compañía estadounidense abrirá una nueva oficina de 3.000 metros cuadrados*
* *La inversión es de 12 millones de euros y estará ejecutada en 2024*

EL PAÍS

SEMICONDUCTORES >

El centro de preproducción de chips de Cataluña: un salto tecnológico para el que ya hay una red

El impulso de esta planta, que abrirá en 2026 con 200 empleados y supondrá una inversión de 360 millones de euros, quiere ser una pieza clave para avanzar en la soberanía europea en semiconductores

CincoDías

Compañías Mercados Economía Mi Dinero Fortuna / Cotizaciones

Compañías

TECNOLOGÍA >

Cisco abrirá en Barcelona su primer centro de diseño de microchips en Europa

Una operaria mueve un carro a través de una de las instalaciones de NXP en Europa. REMKO DE WAAL / AFP

El gigante de los chips NXP busca crecer en España

Sella alianzas en Barcelona y se lanza a captar fondos del Perte

- Què?

Dades generals

- Màster interuniversitari (UPC, UB, UAB, URV, CNM) de nova creació
- Màster oficial, verificat Setembre 2023
- Anglès
- 60 crèdits, 1 any
- 2 branques d'especialitat: Disseny de CIs i Fabricació de CIs
- Titulacions d'accés: Enginyeria Electrònica i Física (+altres Eng.)
- Campus d'impartició: Campus de Barcelona (Campus Nord) +
  Campus de Bellaterra (UAB)
- Universitat i centre coordinador/gestor: UPC, ETSETB
- INICI: setembre de 2024
- PREINSCRIPCIÓ: a partir de 1 de març de 2024

SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (60 ECTS): UPC – Universidad Responsable y Coordinadora

20 ECTS compulsory common subjects

Microelectronic Technologies and Processes (6)
Microelectronic Design (6)
Innovation, Entrepreneurship & leadership (6)
Seminars on microelectronic industry and Advanced research (2)

18 ECTS compulsory IC Manufacturing branch subjects

Semiconductor Devices (6)
Semiconductor Facilities & Device Manufacturing (6)
Packaging, Characterization and Reliability (6)

18 ECTS compulsory IC Design branch subjects

Analog IC Design (6)
SoC Design & Verification (6)
Integrated Circuits Physical Design (6)

elective IC Manufacturing branch subjects
12 ECTS, 3 subjects to be elected

Material Characterization (4)
Integrated Photonics (4)
Power devices & Systems (4)
Microsensors (4)
Emerging Technologies for Computing (4)
Flexible & Printed Electronics (4)

elective IC Design branch subjects
12 ECTS, 3 subjects to be elected

RF IC design (4)
ASIC design techniques for highly secure systems (4)
Advanced IP core design (4)
Integrated Sensors and Circuits for Imagers & Radiation Detectors (4)
Mixed Signal IP Design (4)
Power Management Circuits in ASICS (4)

Master Thesis (10)

20 ECTS compulsory

Description of subjects

Microelectronic Technologies and Processes : \Semiconductor Device Theory \Introduction to microelectronic technologies\ CMOS process design kit (PDK) \ Basic characterization techniques \Introduction to Clean room facilities-

Microelectronic design: IC design methodologies, development stages and EDA tools; technological alternatives (SoC, IPs, FPGAs, uP,….); MOSFET basic behaviour and compact modelling. Basic CMOS circuits (digital and analog). Layouts, tapeout and backend processing.

Innovation, Entrepreneurship & leadership : Technology transfer in R+D+I schemes. Evaluation of innovative ideas, business models and value propositions; risk assessment for spin off / start up ventures. Team Work and distributed leadership. Scientific and business communication. Ethic commitment: economic, social and environmental sustainability, and Sustainable Development Goals.

Seminars on microelectronic industry and Advanced research : State of the art seminars on actual industrial advances and forecast production. Talks about cutting edge research as well as historical perspective of the evolution of microelectronics and its societal impacts.

18 ECTS compulsory Manufacturing ICs

Description of subjects

Semiconductor Devices: \MOS field effect transistor physics \FETs until 22nm node \FET beyond 22nm node \Transport in low dimensional systems

Semiconductor Facilities and Device Manufacturing: Principles and performance of Controlled Environment and/or Clean Room facilities. Design rules for Clean Rooms, cleaning, maintenance and contamination control protocols, and good practices when working in this environment. Quality assessment through the fabrication line. Pilot training course where the student will be involved in the production and characterization of a NMOS device.

Packaging, Characterization and Reliability: Chip packaging, heteregeneous integration. Electrical characterization. Reliability and yield.

18 ECTS compulsory IC Design branch subjects

Description of subjects

Analog and Mixed Signal IC design: /Small-signal models and biasing. Basic amplifiers. Differential Amplifier. Operational amplifiers. Mixed-signal CMOS circuit design techniques for analog frontends (AFEs) and data converters (ADC and DAC). Low power techniques for AFE's. EDA Tools

High Level Digital Design & System Verification: High level hardware description languages. High level digital synthesis. Hardware/Software Interfaces. Logic Synthesis and Verification tools

Integrated Circuits Physical design: Computer design Flow, from RTL to GDS. Related computer Aided Tools. Floorplanning and Place and routing. Device models and corners. Pre and post-layout simulation and verification. Time constraints. . Power evaluation, power constraints. Thermal models. Power and Switching noise. Compensation techniques. Reliability issues. Test of digital circuits. Design sign off.

12 ECTS optional subjects (1/2)

Description of subjects

Material Characterization: Practical view of analytical instrumentation for material characterization, focussed on silicon and other relevant semiconductor, homo- and heterostructures and relevant metallisations and insulations of Ics./ Structural techniques/Spectroscopies/Microscopies. Lab on quantification

Integrated Photonics: /Photonics materials and components (waveguides, beam splitters, grating couplers, emitters, integrated photonic circuits, etc.) /Radiation detectors (2D and 3D detectors, detectors for harsh environments, particle detectors for HEP, dosimetry and medical applications, radiation damage, etc.)/

Power devices & Systems: Power devices (Power Diodes, Power Bipolar Junction Transistors (BJT), Power MOS Field Effect Transistors (MOSFET), Insulated Gate Bipolar Transistors (IGBT), Wide-bandgap semiconductors (SiC, GaN, diamond...).

Emerging Technologies for Computing:\Beyond CMOS (Single electron transistors, 2D transistors) \Neuromorphics (ReRAM, Computation in Memory, Stochastic computation) \ Quantum processing devices

Sensors for IOT: More than Moore, Micro/Nanosystems, Energy harvesting, Environmental sensors, Low power AFE, wireless communications,

12 ECTS optional subjects (2/2)

Description of subjects

RF IC design: / Front-end architectures for communication systems. System-level and circuit-level parameters. Communication standard to circuit specs. Case study: The Bluetooth receiver design. /CMOS technology for RF. MOS models for RF. CMOS LNA, VCOs, PA, PLL and frequency synthesizers. Technological alternatives MMICs. Simulations tools for RF: ADS, SpectreRF, Ansys….

Advanced IP core design: Von-Neumann Architecture and performance. Linearly pipelined processor. Datapath. Structural, Control and Data Hazards. Techniques to increase the number of instructions executed per unit of time Static code planification.. Techniques to reduce the effective latency of memory Caches. Branch Prediction and Exception Handling. Static and Dynamic Branch Prediction. Speculative Execution, Precise Exception handling. Superscalar and out-of-order processors Register Renaming. Out-of-Order handling.

Design of digital communication circuits: Network Processors Design, Architectures, Memory systems. Queue systems. Advanced Switcher VLSI design. Serdes. Advanced data transfer mechanisms.

- Com?

Dades generals

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
- Microelectronic Technologies and Processes (6) - Microelectronic Design (6)						Evaluation, Seminars and Campus Activities (ecosystem)		- Semiconductor Devices (6) - Semiconductor Facilities & Device Manufacturing (6) - Packaging, Characterization and Reliability (6)						Evaluation, Seminars, Campus Activities (ecosystem) Master matching activities	
								- Analog IC Design (6) - SoC Design & Verification (6) - Integrated Circuits Physical Design (6)							

Mandatory subject
Technology branch Mandatory subject
Design branch Mandatory subject

First Semester

(16 week academic period)

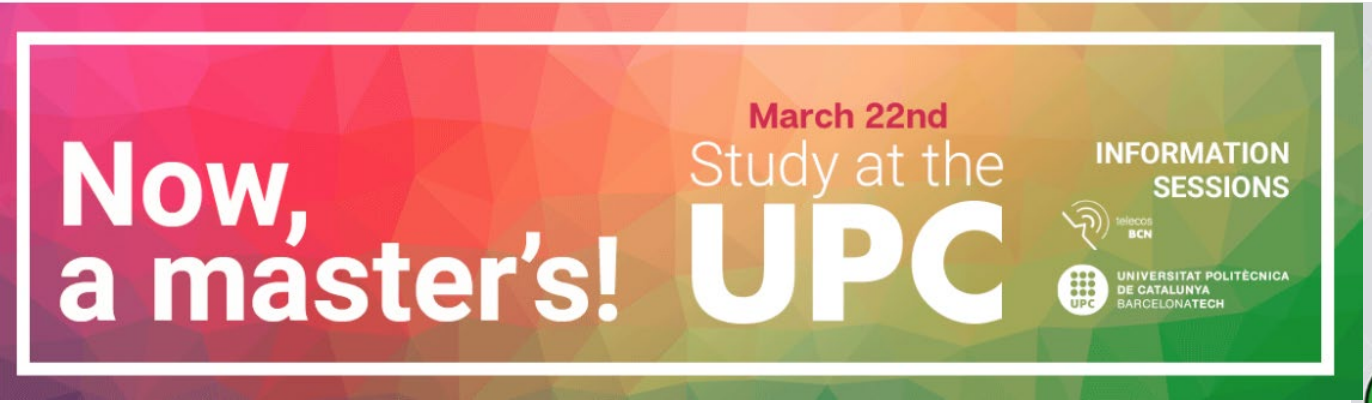
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
- Material Characterization (4) - Integrated Photonics (4) - Power devices & Systems (4) - Microsensors (4) - Emerging Technologies for Computing (4) - Flexible & Printed Electronics (4)						Evaluation, Seminars, Campus Activities (ecosystem) Master definition activities		- Master Thesis (10)					- Innovation, Entrepreneurship & Leadership (6)		Master Thesis presentation week And Closing master activities
- RF IC design (4) - ASIC design techniques for highly secure systems (4) - Advanced IP core design (4) - Integrated Sensors and Circuits for Imagers & Radiation Detectors (4) - Mixed signal IP design (4) - Power Management Circuits in ASICS (4)															

Mandatory subject –
Mandatory subject – According with your supervisor
Technology branch Elective subject (minimum 3 subjects)
Design branch Elective subject (minimum 3 subjects)

Evaluation and other activities. Seminars on microelectronic industry and advanced research (2) will hold mainly during these periods.

Second Semester

(16 week academic period)



Preenrolment video tutorial: Everything you need to know about admission and enrolment

TUTORIAL Masters Pre-Enrolment

UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Escola Tècnica Superior d'Enginyeria de Telecomunicació de Barcelona

PRE-ENROLMENT Deadlines Fall Semester 2024-2025

(to begin classes in September 2024)

From **March 1, 2024**
to July 1, 2024

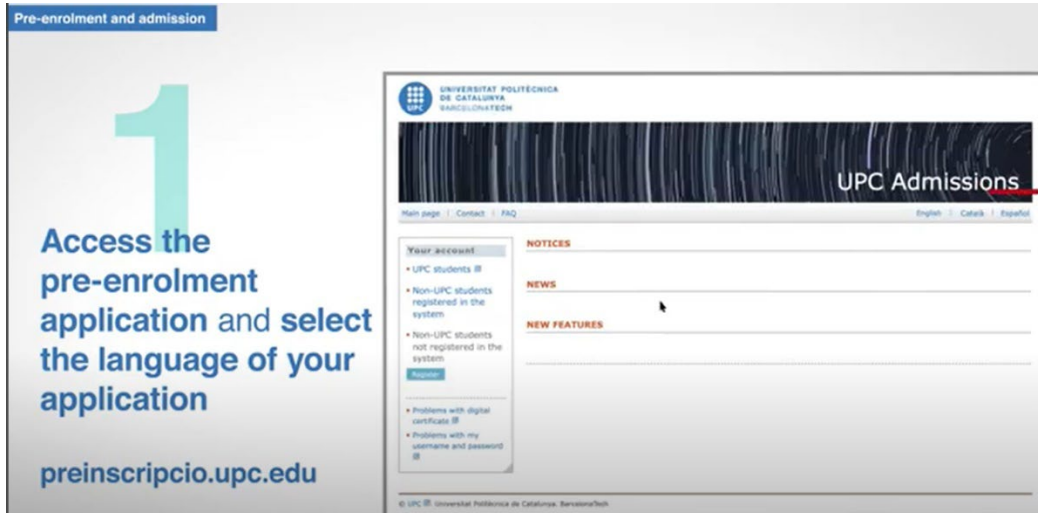
Check the places available for the spring term in this link :MASTERS. Programs and offered places

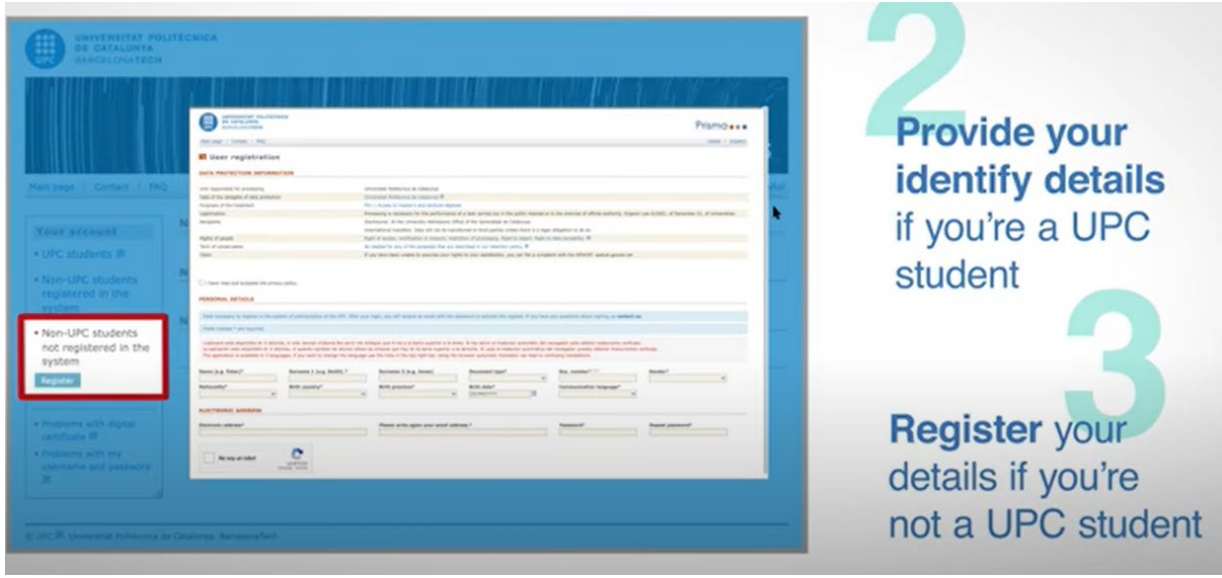
- ✓ Admitted student's resolution to be published end of July, 2024.
- ✓ Classes begin : **September 2024**
  Calendaris Lectius

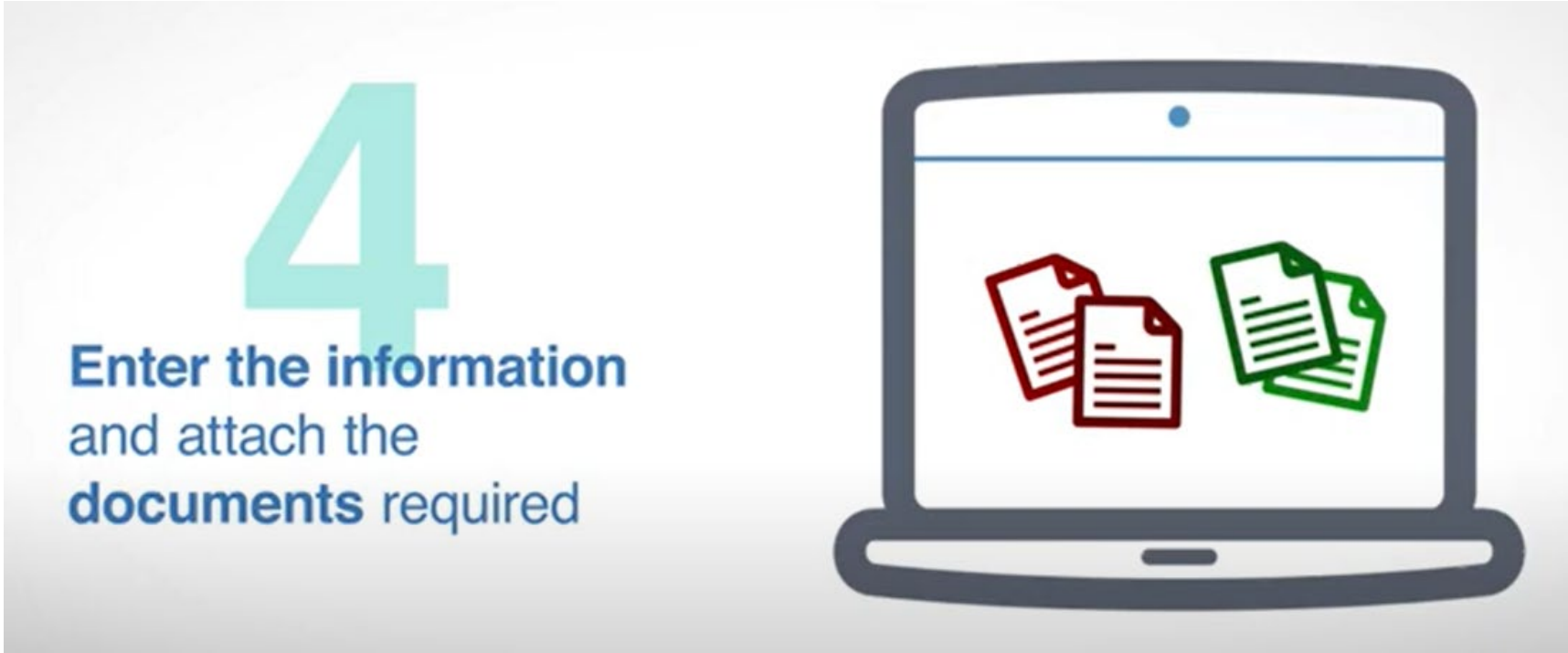
MASTERS. Pre-enrolment.

Master's degree in Semiconductor Engineering and Microelectronic Design

Preenrolment video tutorial: Everything you need to know about admission and enrolment







Required Documents to upload

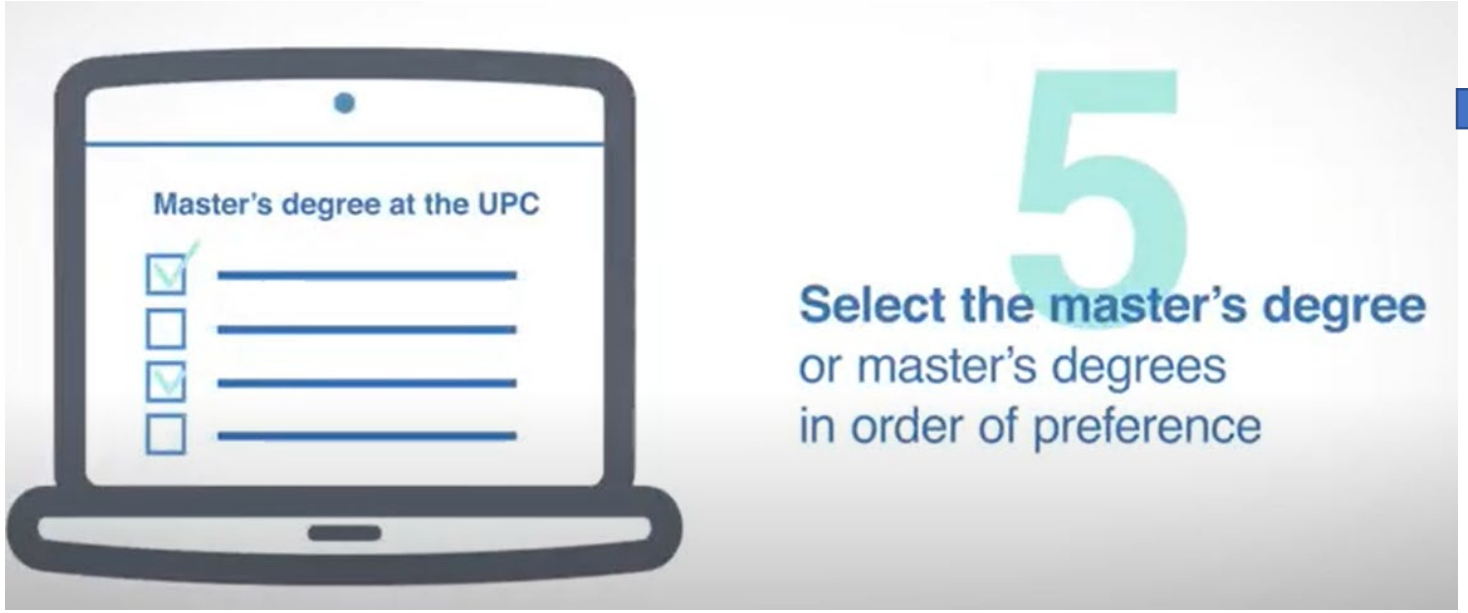
The documents you will have to upload depend on where you have earned the degree that qualifies you to enroll in the master's degree.

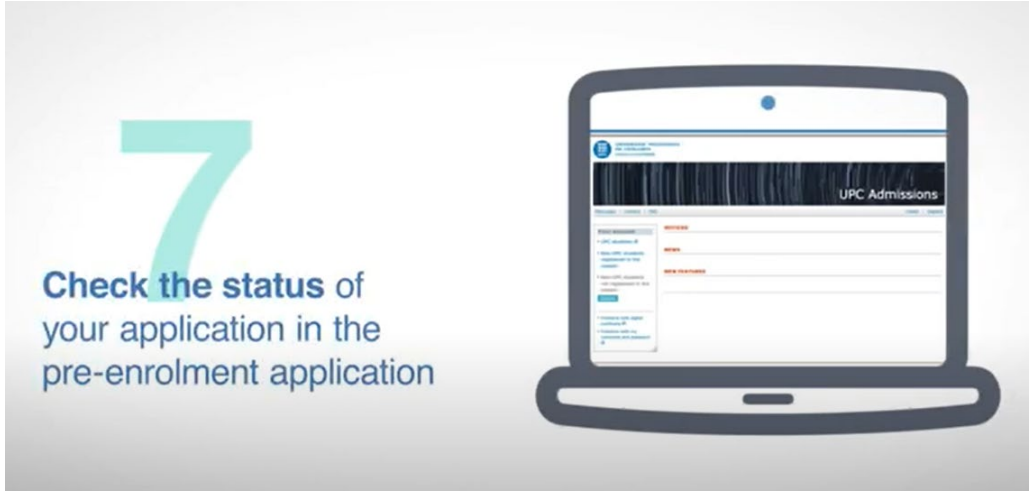
UPC	any other **PUBLIC UNIVERSITY in Spain**	**FOREIGN UNIVERSITIES**
ID (only foreign students)	ID (only foreign students)	Passport
B.2.2 ENGLISH CERTICATE (1)	B.2.2 ENGLISH CERTICATE (1)	B.2.2 ENGLISH CERTICATE (1)
Curriculum vitae	Curriculum vitae	Curriculum vitae
	TRANSCRIPT OF RECORDS (2)	**Legalized and translated TRANSCRIPT OF RECORDS** (2)
	BACHELORS DIPLOMA (2)	**Legalized and translated BACHELORS DIPLOMA** (2)
		Official certificate of the EQUIVALENCES to the rating system of Spanish universities
		Subjects description: Document or link to the course description of the subjects in the transcript of records.

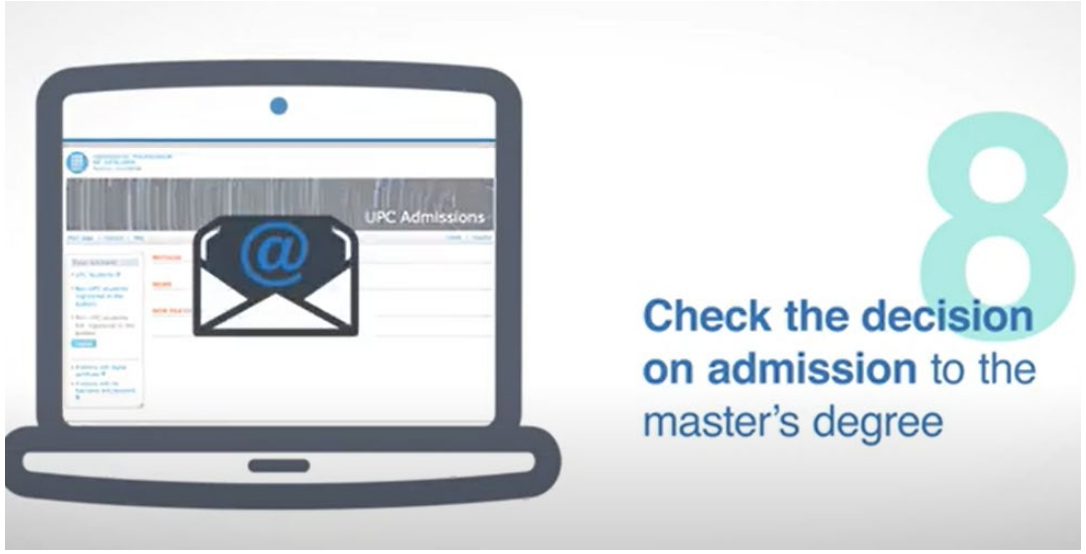
(1) Consult the language certificates table by language to prove you meet the B2 requirement in the Catalan version of the website: http://www.upc.edu/slt/ca/certifica/taulaB2#taula

(2) It is mandatory that you upload the **CERTIFIED DIGITAL ACADEMIC DOCUMENTS** (that include a verification code or link to be used on the website of the university to verify authenticity and content. The original handwritten signed documents cannot be verified.)

Preenrolment video tutorial: Everything you need to know about admission and enrolment

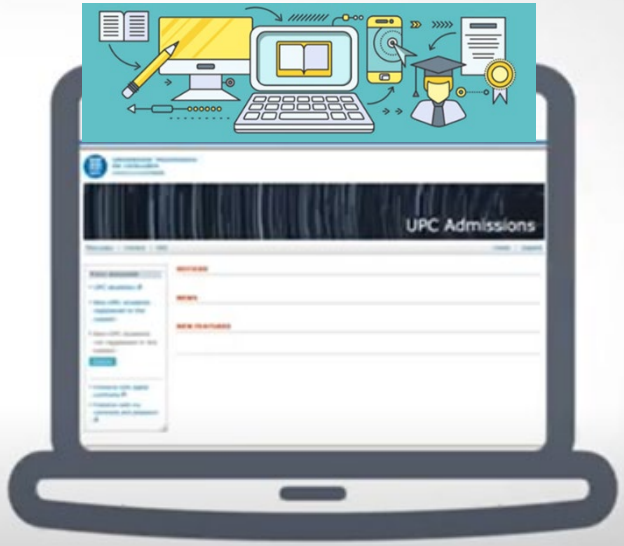






7

Check the status of your application in the pre-enrolment application



ETSETB Masters: Information Sessions

Master informative sessions

In-Person

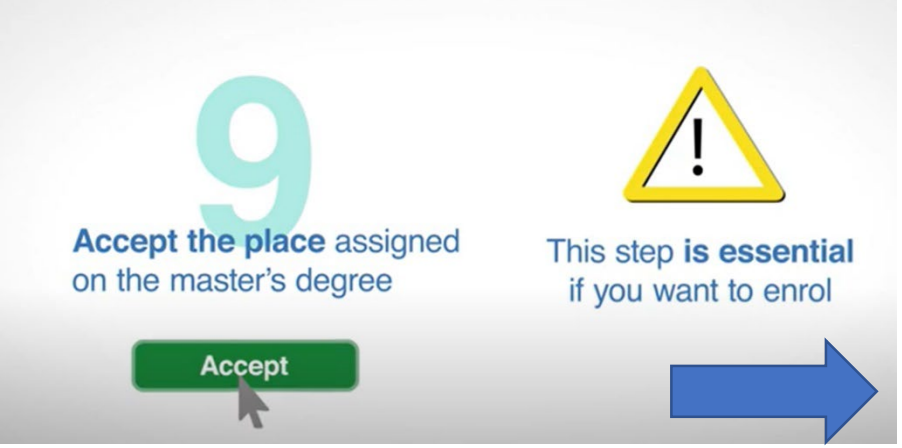
How do we assist you?

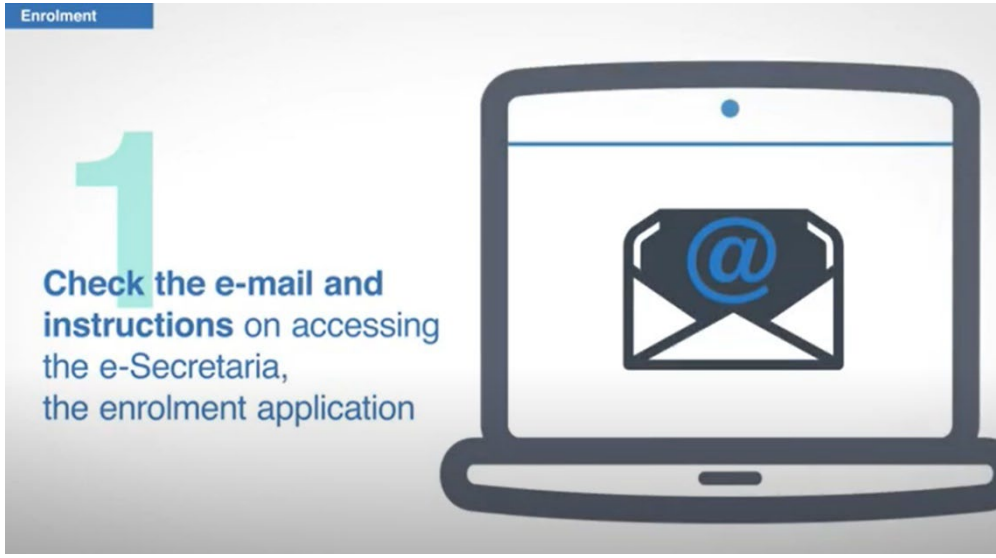
00-34- 93 4016750

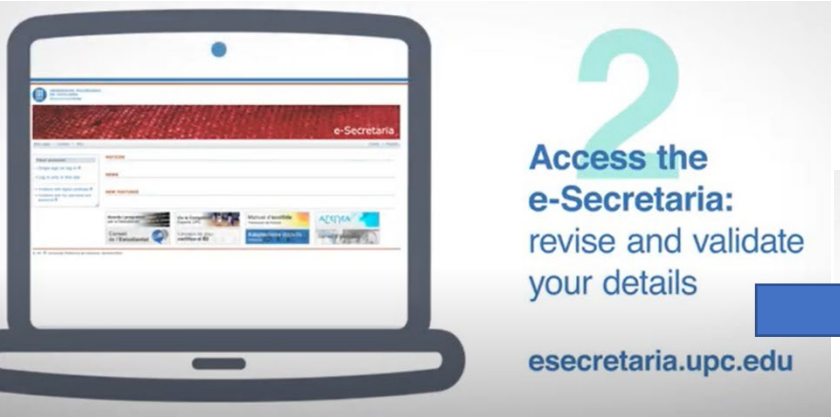
masters.etsetb@upc.edu

PRIOR APPOINTMENT

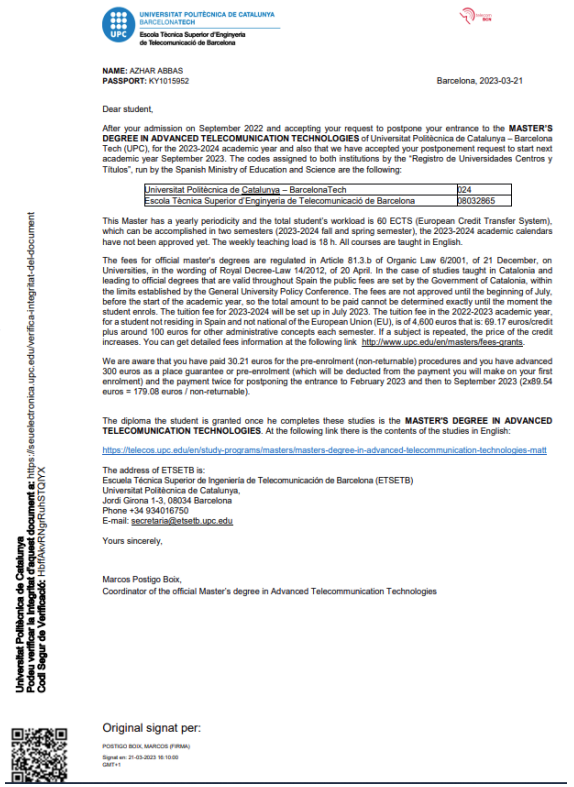
Only available on the enrolment day







+ to request the Admission Letter mandatory for the VISA procedures



UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Escola Tècnica Superior d'Enginyeria de Telecomunicació de Barcelona

NAME: AZHAR ABBAS
PASSPORT: KY1015952

Barcelona, 2023-03-21

Dear student,

After your admission on September 2022 and accepting your request to postpone your entrance to the **MASTER'S DEGREE IN ADVANCED TELECOMUNICATION TECHNOLOGIES** of Universitat Politècnica de Catalunya – Barcelona Tech (UPC), for the 2023-2024 academic year and also that we have accepted your postponement request to start next academic year September 2023. The codes assigned to both institutions by the "Registro de Universidades Centros y Títulos", run by the Spanish Ministry of Education and Science are the following:

Universitat Politècnica de Catalunya – BarcelonaTech	024
Escola Tècnica Superior d'Enginyeria de Telecomunicació de Barcelona	08032865

This Master has a yearly periodicity and the total student's workload is 60 ECTS (European Credit Transfer System), which can be accomplished in two semesters (2023-2024 fall and spring semester), the 2023-2024 academic calendars have not been approved yet. The weekly teaching load is 18 h. All courses are taught in English.

The fees for official master's degrees are regulated in Article 81.3.b of Organic Law 6/2001, of 21 December, on Universities, in the wording of Royal Decree-Law 14/2012, of 20 April. In the case of studies taught in Catalonia and leading to official degrees that are valid throughout Spain the public fees are set by the Government of Catalonia, within the limits established by the General University Policy Conference. The fees are not approved until the beginning of July, before the start of the academic year, so the total amount to be paid cannot be determined exactly until the moment the student enrols. The tuition fee for 2023-2024 will be set up in July 2023. The tuition fee in the 2022-2023 academic year, for a student not residing in Spain and not national of the European Union (EU), is of 4,600 euros that is: 69.17 euros/credit plus around 100 euros for other administrative concepts each semester. If a subject is repeated, the price of the credit increases. You can get detailed fees information at the following link: http://www.upc.edu/en/masters/fees-grants.

We are aware that you have paid 30.21 euros for the pre-enrolment (non-returnable) procedures and you have advanced 300 euros as a place guarantee or pre-enrolment (which will be deducted from the payment you will make on your first enrolment) and the payment twice for postponing the entrance to February 2023 and then to September 2023 (2x89.54 euros = 179.08 euros / non-returnable).

The diploma the student is granted once he completes these studies is the **MASTER'S DEGREE IN ADVANCED TELECOMUNICATION TECHNOLOGIES**. At the following link there is the contents of the studies in English:

https://telecos.upc.edu/en/study-programs/masters/masters-degree-in-advanced-telecommunication-technologies-matt

The address of ETSETB is:
Escuela Técnica Superior de Ingeniería de Telecomunicación de Barcelona (ETSETB)
Universitat Politècnica de Catalunya,
Jordi Girona 1-3, 08034 Barcelona
Phone +34 934016750
E-mail: secretaria@etsetb.upc.edu

Yours sincerely,

Marcos Postigo Boix,
Coordinator of the official Master's degree in Advanced Telecommunication Technologies

Universitat Politècnica de Catalunya
Podeu verificar la integritat d'aquest document a: https://seuelectronica.upc.edu/verifica-integritat-del-document
Codi Segur de Verificació: HdrfAwRNgRuINSTOYX

Original signat per:

POSTIGO BOIX, MARCOS (FIRMA)
Signat en: 21-03-2023 16:10:00
GMT+1

“Ministerio de Educación” Scholarship

NEW !! Deadline for submitting applications scholarship from the Ministry of Education 2023/24

2024-2025 deadlines :

To be updated but usually from march to may.

https://www.upc.edu/sga/ca/Beques/BequesEstudi/BecaM

Portal "Becas de Educación" del Ministerio de Educación

The information about grants and financial aid is available in this link https://www.upc.edu/en/masters/fees-grants
Important: they are only eligible those students that are Spanish or have been paying taxes in Spain as a resident.

As a master's degree student, you can apply for Ministry of Education, Culture and Sport (MECD) grants to cover credits enrolled for the first time and if your income and academic performance make you eligible. You can also apply for EQUITAT grants from Catalonian government, if you are a student of a qualifying master's degree (MET).

No grant are available for foreign students, they should request a grant in their home countries check with general services if there is an agreement with the UPC.

ETSETB-Àrea de Gestió Acadèmica

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Màster en

Enginyeria de Semiconductors i Disseny Microelectrònic

Comitè acadèmic:

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Dr. Xavier Muñoz, Centre Nacional de Microelectrònica

Dr. Antonio Rubio, Universitat Politècnica de Catalunya

Dr. Albert Cirera, Universitat de Barcelona

Dr. Benjamín Íñiguez, Universitat Rovira i Virgili